4/19/04

INFORMATION DISCLOSURE CITATION PTO-1449	Atty Docket 054355/0039380	Serial No. 10/828,547
	Applicant **Van Ginneken**	
	Filing Date **April 19, 2004**	Group Art Unit 2825

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
VS	5,282,148	01/25/94	Poirot et al.	364		
	5,475,605	12/12/95	Lin	364		
	5,537,330	07/16/96	Damiano et al.	364		
	5,168,455	12/01/92	Hooper	364		
	5,237,514	08/17/93	Curtin	364		
	5,392,221	02/21/95	Donath et al.	364		
VS	5,397,749	03/14/95	Igarashi	437		

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EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation Yes	Translation No
VS	0 610 626 A2	08/17/94	EP				

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VS	K.Keutzer, "DAGON: Technology Binding and Local Optimization by DAG Matching, *Proc.of the 24th ACM/IEEE Design Automation Conference*, Miami Beach, Fl (June 1987), pp. 341-347, IEEE Computer Society Press 1987.
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EXAMINER	VUTHE SIEK	DATE CONSIDERED	3/8/06

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in

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	Applicant **Van Ginneken**	
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U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
VS	5,402,357	03/28/95	Schaefer, et al.	364		
	5,404,312	04/04/95	Tawada	364		
	5,426,591	06/20/95	Ginetti, et al.	364		
	5,490,268	02/06/96	Matsunaga	395		
	5,550,748	08/27/96	Xiong	364		
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	5,689,432	11/18/97	Blaauw et al.	716		
VS	6,453,446	09/2002	Van Ginneken	716		

EXAMINER VUTHE SIEK	DATE CONSIDERED 3/10/07

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PATENT & TRADEMARK OFFICE

Form PTO-1449 (Substitute)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	Attorney Docket Number MDAI.001US3	Application/Patent Number 10/828,547
	INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant/Patent Owner Lukas P.P.P. van Ginneken	
		Filing/Issue Date April 19, 2004	Group Art Unit 2825

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Examiner Initial		Patent Number	Issue Date	First Named Inventor	Class	Subclass	Filing Date

U.S. PATENT PUBLICATIONS

Examiner Initial		Patent Application Publication Number	Publication Date	Applicant

PENDING U.S. PATENT APPLICATIONS

Examiner Initial		Application Number	Filing Date	First Named Inventor	Petition to Expunge? Yes | No

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Publication Date	Country	Class	Subclass	Translation Yes | No

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16	Camposano, Raul	"The Quarter Micron Challenge: Integrating Physical and Logic Design"	*ISPD '97*	1997

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	Chang, Shih-Chieh	"Layout Driven Logic Synthesis for FPGAs"	*31ST ACM/IEEE Design Automation Conference*	1994
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	Chen, Wei	"Gate Sizing with Controlled Displacement"	*Department of Electrical Engineering –System* *University of Southern California, Los Angeles*	No date
	Chen, Wei	"Simultaneous Gate Sizing and Placement"	*Department of Electrical Engineering – System* *University of Southern California, Los Angeles*	No date
	Chuang, Weitong	"Delay and Area Optimization for Compact Placement by Gate Resizing and Relocation"	*Association for Computing Machinery*	1994
	Cong, Jason	"An Efficient Approach to Simultaneous Transistor and Interconnect Sizing"	*Department of Computer Science* *University of California, Los Angeles*	1996
	Cong, Jason, Cheng-Kok Koh and Kwong-Shing Leung ["Cong 1996A"]	"Simultaneous Buffer and Wire Sizing for Performance and Power Optimization"	ISLPED	1996

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V5	Otten, Ralph H. J. M., Lukas P. P. P. van Ginneken ["Otten 1996A"]	"SPEED: new paradigms in design for performance"	*Presentation Slides*	November 13, 1996
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	Rabaey, Jan M. ["Rabaey 1996"]	---	*Digital Integrated Circuits: A Design Perspective*	1996 (©Prentice Hall)
	Sarabi, Andisheh	"A Comprehensive Approach to Logic Synthesis and Physical Design for Two-Dimensional Logic Arrays"	*31st ACM/IEEE Design Automation Conference*	1994
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V3	Shah, Jatan	"Wiresizing with Buffer Placement and Sizing for Power-Delay Tradeoffs"	*Department of Electrical and Computer Engineering* *Iowa State University*	No date

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√	Singh, Kanwar Jit and Alberto Sangiovanni-Vincentelli ["Singh 1990"]	"A Heuristic Algorithm for the Fanout Problem"	*27th Design Automation Conference*	1990
	Stenz, Guenter	"Timing Driven Placement In Interaction with Netlist Transformation"	*ISPD '97*	1997
	Stok, Leon	"BooleDozer: Logic Synthesis for ASICs"	*IBM*	1996
	Sutherland, Ivan E. and Robert F. Sproull ["Sutherland 1991"]	"Logical Effort: Designing for Speed on the Back of an Envelope"	*Proceedings of the 1991 University of California, Santa Cruz Conference on Advanced Research in VLSI, Santa Cruz, CA*	1991
	Vaishnav, Hirendu	"Minimizing the Routing Cost During Logic Extraction"	*32nd ACM/IEEE Design Automation Conference*	1995
	Vaishnav, Hirendu	"Routability-Driven Fanout Optimization"	*30th ACM/IEEE Design Automation Conference*	1993
	van Ginneken, Lukas P. P. P. ["van Ginneken 1990A"]	"Buffer Placement in Distributed RC-tree Networks for Minimal Elmore Delay"	International Symposium on Circuits and Systems, 1990	May 1-3, 1990
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V5	United States District Court for the Northern District of California	Amended Order RE: Claim Construction of United States Patent Nos. 6,453,446, 6,725,438 and 6,378,114		August 23, 2005
Examiner	VUTHE SIEK		Date Considered	3/8/06

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*1 = Copy not submitted because it was submitted in prior application SN / , filed , 20 , relied on under 35 USC §120.
*2 = Copy not submitted because it was submitted in prior application SN / , filed , 20 , relied on under 35 USC §120.

SF1:599560.1

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U.S. Department of Commerce, Patent and Trademark	Atty. Docket No.	Application No.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	MDAI.001US3	10/828,547
	Applicant	Conf. No.
(Use several sheets if necessary)	Lukas P.P.P. van Ginneken	3884
(Form PTO-1449)	Filing Date	Art Group
	April 19, 2004	2825

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate

U.S. Published Patent Application Documents

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Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

V5	1	Synopsis, Inc. vs. Magma Design Automation, Inc., C04-03923 MMC, "Defendant Magma Design Automation, Inc.'s Answer to Plaintiff Synopsys, Inc.'s Third Amended Complaint and Counterclaims, Demand for Jury Trial," filed in the U.S. District Court, Northern District of California, San Francisco Division on September 2, 2005, 38 pages.
	2	Synopsis, Inc. vs. Magma Design Automation, Inc., C04-03923 MMC, "Declaration of Lukas van Ginneken," filed in the U.S. District Court, Northern District of California, San Francisco Division on July 29, 2005, 8 pages.
	3	Synopsis, Inc. vs. Magma Design Automation, Inc., C04-03923 MMC, "Videotaped Deposition Upon Oral Examination of Lukas van Ginneken, PhD, Volume I," dated April 26, 2005, 58 pages.
	4	Synopsis, Inc. vs. Magma Design Automation, Inc., C04-03923 MMC, "Videotaped Deposition Upon Oral Examination of Lukas van Ginneken, PhD, Volume II," dated April 27, 2005, 58 pages.
V5	5	Synopsis, Inc. vs. Magma Design Automation, Inc., C04-03923 MMC, "Third Amended Complaint for: 1. Patent Infringement; 2. Breach of Contract; 3. Inducing Breach of Contract/Interference With Contractual Relations; 4. Fraud; 5. Conversion; 6. Unjust Enrichment/Constructive Trust and; 7. Unfair Competition, Demand for Jury Trial," filed in the U.S. District Court, Northern District of California, San Francisco Division on August 3, 2005, 37 pages.

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VS	1	Berkelaar et al., "Gate Sizing in MOS Digital Circuits With Linear Programming", The European Design Automation Conference, March 12-15, 1990, pp. 217-221.
	2	Chuang et al., "Delay and Area Optimization for Discrete Gate Sizes Under Double-Sided Timing Constraints", Proc. IEEE 1993 Custom Integrated Circuits Conf., pp. 1-4.
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U.S. Published Patent Application Documents

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Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
VJ	1	EP 0 610 626 A2	17/8/94	Europe			X	

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

VJ	2	Canadian Patent Office, Office Action, mailed October 5, 2005 in Canadian Application No. 2,317,538, 4 pages.

Examiner	VUTHE SIEK	Date Considered	3/8/06

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